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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,012	04/07/2004	Glenn G. Daves	FIS920010103US2	3011
29371	7590	01/27/2005	EXAMINER	
CANTOR COLBURN LLP			ROMAN, ANGEL	
55 GRIFFIN ROAD SOUTH			ART UNIT	
BLOOMFIELD, CT 06002			PAPER NUMBER	

2812

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/709,012	Applicant(s) DAVES ET AL.	
	Examiner Angel Roman	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 April 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>04/07/04</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: The Cross reference To Related Applications section should be updated to include the parent application patent number --6,762,489--.

Appropriate correction is required.

Drawings

2. Figure I should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 2 is objected to because of the following informalities: In line 5, "said x-axis" should be replaced with --an x-axis--; and in line 9, "said y-axis" should be

replaced with --a y-axis-- since there is no antecedent basis for these limitations in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Corisis et al. U.S. Patent 6,072,233 A.

Regarding claim 1, Corisis et al. discloses a method for implementing a wiring translation in chip carrier module between corresponding points in a first grid and a second grid, the points in the first grid defining a first plane the points in the second grid defining a second plane, the second plane lying substantially parallel to the first plane (see figure 4), the method comprising; connecting the first grid to a first translation layer (30) within the module, said first translation layer (30) translating the points in the first grid in a first direction (see figure 3), and connecting a second translation layer between said first translation layer and the second grid, said second translation layer translating the points in the first grid in a second direction, said second direction being orthogonal to said first direction (see figure 5).

Regarding claim 2, Corisis et al. teaches a first translation layer (30) configured to include a first plurality of signal interconnects (20), each of said first plurality of signal

interconnects (20) having a jog line elongated along an x-axis direction (see figure 3); and said second translation layer is configured to include second plurality of signal interconnects, wherein each of said second plurality of signal interconnects have a jog line elongated along a y-axis direction (see figure 5).

Regarding claim 3, Corisis et al. discloses each of said jog lines in said first plurality of signal interconnects are disposed between an upper via contact and a lower via contact in said first translation layer (see figure 3); and each of said jog lines in said second plurality of signal interconnects are disposed between an upper via contact and a lower via contact in said second translation layer (see figure 5).

Regarding claim 4, Corisis et al. discloses each individual upper via contact in said first translation layer is in electrical communication with a corresponding point in the first grid; each individual lower via contact in said first translation layer is in electrical communication with a corresponding upper via contact in said second translation layer; each individual lower via contact in said second translation layer is in electrical communication with a corresponding point in the second grid; and each signal via in said first plurality of signal vias are in electrical contact with corresponding individual signal vias in said second plurality of signal vias (see figure 11).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis et al. U.S. Patent 6,072,233 A.

Corisis et al. is applied as above but lacks anticipation on disclosing a second grid comprising a logic service terminal. Corisis et al. discloses the first and second grid comprising C4 grids and also discloses using the second grid as a terminal grid to connect to other modules (see figure 11), therefore it would have been obvious to a

person having ordinary skills in the art at the time the invention was made to form the second grid of Corisis et al. to function as a logic service terminal since it would translate the grids as describe in Corisis et al..

Allowable Subject Matter

10. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record either singularly or in combination failed to anticipate or render obvious the limitations of configuring a plurality of power buses in the first translation layer disposed along the x-axis direction and configuring a second plurality of power buses in the second translation layer in the y-axis direction as required by claim 5.

Conclusion


12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shi et al., Weekly et al., Bhatia et al., Kado et al., Ho et al., Frech et al., Mohsen and Feinberg et al. disclose methods for implementing wiring translation in chip carrier modules.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
January 21, 2005


MICHAEL S. LEBENTRITT
PRIMARY EXAMINER
